

## N-Channel Enhancement-Mode MOS Transistor

### Product Summary

$V_{(BR)DSS}$ Min (V)	$r_{DS(on)}$ Max ( $\Omega$ )	$V_{GS(th)}$ (V)	$I_D$ (A)
200	11	0.8 to 3.0	0.085

### Features

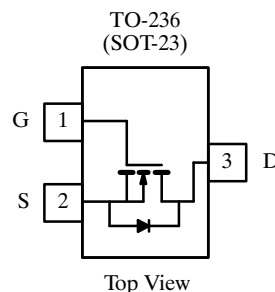
- Low On-Resistance: 9.5  $\Omega$
- Secondary Breakdown Free: 220 V
- Low Power/Voltage Driven
- Low Input and Output Leakage
- Excellent Thermal Stability

### Benefits

- Low Offset Voltage
- Full-Voltage Operation
- Easily Driven Without Buffer
- Low Error Voltage
- No High-Temperature “Run-Away”

### Applications

- High-Voltage Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Transistors, etc.
- Telephone Mute Switches, Ringer Circuits
- Power Supply, Converters
- Motor Control



Top View

TN2010T (R1)\*

\*Marking Code for TO-236

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	200	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_A = 25^\circ\text{C}$ 0.085	A
		$T_A = 70^\circ\text{C}$ 0.07	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	0.34	W
Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$ 0.2	
		$T_A = 70^\circ\text{C}$ 0.128	
Maximum Junction-to-Ambient	$R_{thJA}$	625	$^\circ\text{C}/\text{W}$
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	$-55$ to $150$	$^\circ\text{C}$

Notes

a. Pulse width limited by maximum junction temperature.

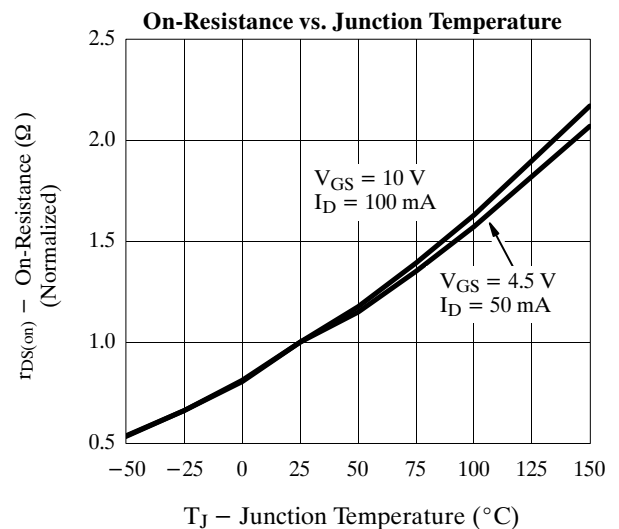
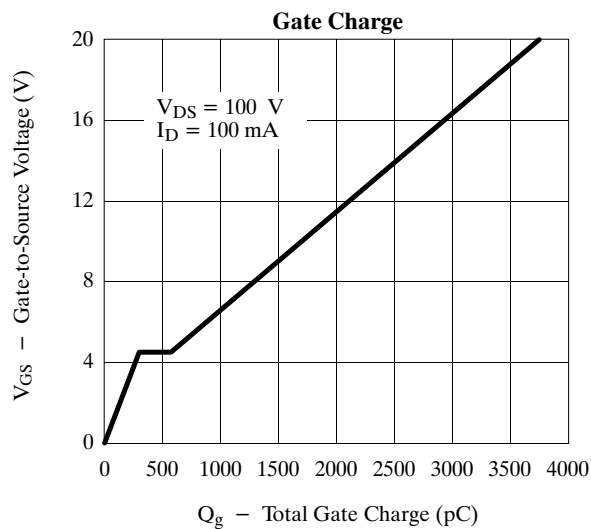
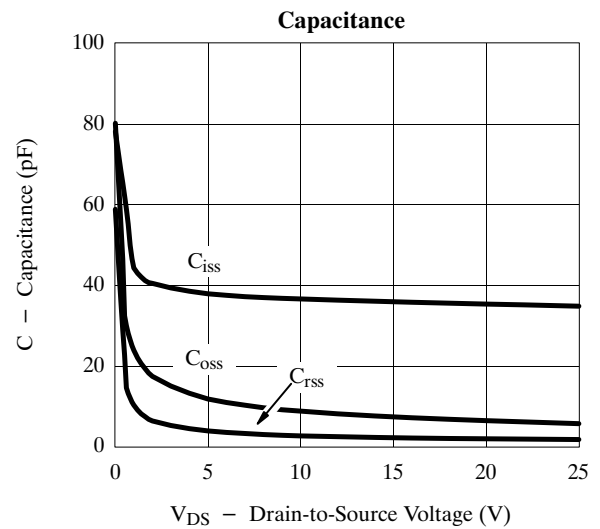
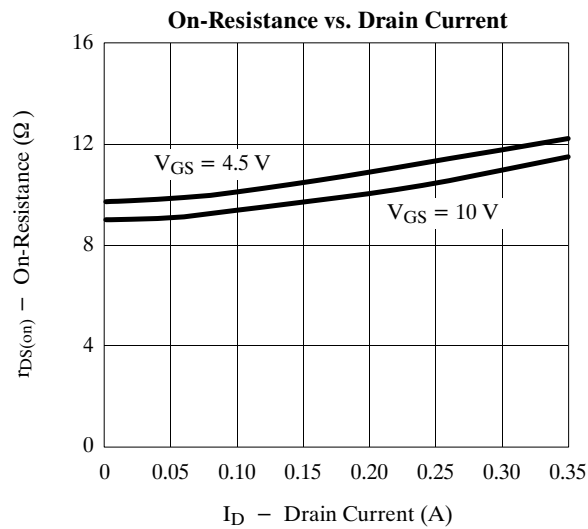
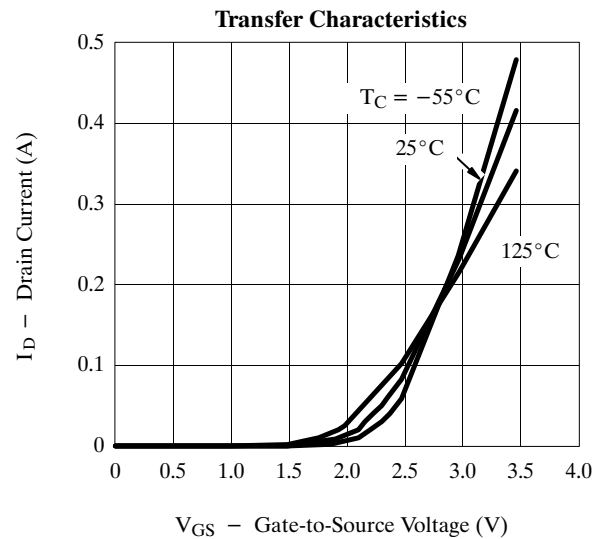
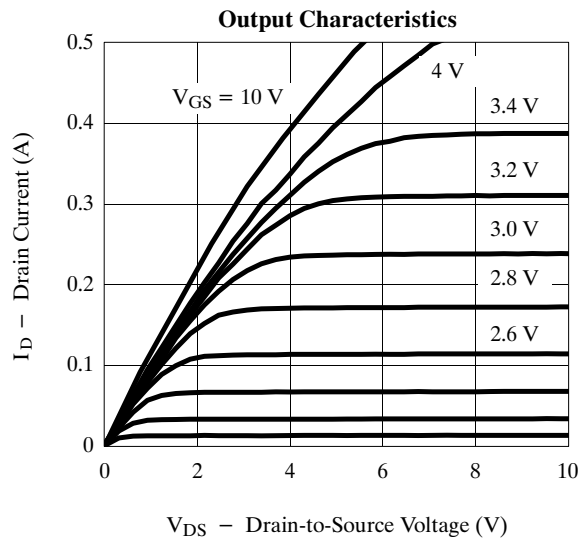
Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ <sup>b</sup>	Max	
Static						
Drain-SourceBreakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 100 μA	200	220		V
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25 mA	0.8	1.6	3.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V			1	μA
		T <sub>J</sub> = −55°C			10	
On-State Drain Current <sup>c</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V	0.3			mA
Drain-Source On-Resistance <sup>c</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.1 A		9.5	11	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.05 mA		10	15	
Forward Transconductance <sup>c</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.1 A		300		mS
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 0.085 A, V <sub>GS</sub> = 0 V		0.8		V
Dynamic						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> ≈ 0.1 A		1750		pC
Gate-Source Charge	Q <sub>gs</sub>			275		
Gate-Drain Charge	Q <sub>gd</sub>			300		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		35		pF
Output Capacitance	C <sub>oss</sub>			6		
Reverse Transfer Capacitance	C <sub>rss</sub>			2		
Switching <sup>d</sup>						
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 60 V, R <sub>L</sub> = 600 Ω I <sub>D</sub> ≡ 0.1 A, V <sub>GEN</sub> = 10 V R <sub>G</sub> = 6 Ω		4		ns
	t <sub>r</sub>			16		
Turn-Off Time	t <sub>d(off)</sub>			16		
	t <sub>f</sub>			45		

## Notes

- a.  $T_A = 25^\circ\text{C}$  unless otherwise noted.  
b. For DESIGN AID ONLY, not subject to production testing.  
c. Pulse test:  $PW \leq 300\text{ }\mu\text{s}$  duty cycle  $\leq 2\%$ .  
d. Switching time is essentially independent of operating temperature.

## Typical Characteristics (25°C Unless Otherwise Noted)



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